REMARKS

Claims 1-3, 7-11, 13, 15-20, 24-26, 29-30 and 33-37 are pending in this application. By this Amendment, claims 1-2, 7, 9-10, 13, 15, 18-19 and 30 are amended and claims 4, 6, 12 and 14 are canceled without prejudice or disclaimer. Various amendments are made for clarity and are unrelated to issues of patentability.

The Office Action rejects claims 1-4, 6-20 24-26, 29-30 and 33-37 under 35 U.S.C. §103(a) over U.S. Patent 5,365,475 to Matsumura et al. (hereafter Matsumura) in view of U.S. Patent 4,901,285 to Sano et al. (hereafter Sano) and U.S. Patent 6,593,799 to De et al. (hereafter De). The rejection is respectfully traversed with respect to the pending claims.

Independent claim 1 recites a first transistor pair and a second transistor pair to couple between the supply voltage line and GROUND, the supply voltage line to receive a first supply voltage when the SRAM memory device is in an ACTIVE mode and to receive a second supply voltage when the SRAM memory device is in a STANDBY mode, the second supply voltage being different than the first supply voltage. Independent claim 1 also recites a first access transistor, a second access transistor, and a bias transistor to couple to a body of one of the transistors of the first transistor pair and to a body of one of the transistors of the second transistor pair, the bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair when the SRAM memory device is in the STANDBY mode. Independent claim 1 also recites that a gate of the bias transistor is coupled to a signal line to receive a STANDBY signal indicative of the STANDBY mode of the SRAM memory device.

The applied references do not teach or suggest at least these features of independent claim 1. More specifically, the applied references do not teach or suggest a supply voltage line to receive a first supply voltage when the SRAM memory device is in an ACTIVE mode and to receive a second supply voltage when the SRAM memory device is in a STANDBY mode, the second supply voltage being different than the first supply voltage.

The Office Action asserts that Matsumura's SRAM mode/ACTIVE mode corresponds to a first mode and Matsumura's ROM mode (storing on data) corresponds to a second mode. However, independent claim 1 specifically relates to an SRAM memory device being in an ACTIVE mode or an INACTIVE mode. Matsumura does not teach or suggest applying different supply voltages to a supply voltage line based on a mode of a SRAM memory device. Matsumura's discussion of a ROM mode does not teach or suggest to receive a second supply voltage when the SRAM memory device is in a STANDBY mode. Matsumura does not teach or suggest the supply voltage line to receive a first supply voltage when the SRAM memory device is in an ACTIVE mode and to receive a second supply voltage when the SRAM memory device is in a STANDBY mode. The other applied references do not teach or suggest these features.

Additionally, Matsumura also does not teach or suggest the claimed supply voltage line. Rather, Matsumura discloses separate voltage lines V1 and V2. Matsumura does not suggest the specific features of the first transistor pair, the second transistor pair and the

claimed supply voltage line. The other applied references do not teach or suggest this feature.

The Office Action (on page 5) states that Matsumura does not disclose the claimed STANDBY mode. The Office Action then relies on Sano's FIGs. 1A, 1B; col. 4, lines 11-13, 36-37 and lines 46-52 as allegedly teaching these features. However, the cited section merely relates to during operation of a ROM 10 while not being read (standby mode). In this circumstance, ROM enable circuitry 62 puts ROM 10 in a pre-charge state. See, for example, col. 4, lines 36-48. This does not teach or suggest when the SRAM memory device is in a STANDBY mode. This also does not relate to a gate of a bias transistor to receive a STANDBY signal indicative of the STANDBY mode of the SRAM memory device.

Further, the Office Action (on page 6) states that Matsumura and Sano do not teach or suggest a bias transistor to apply a forward body bias to the one transistor of the first transistor pair and to the one transistor of the second transistor pair based on STANDBY signal. However, amended independent claim 1 recites when the SRAM memory device is in the STANDBY mode. The Office Action then cites De's FIG. 7, col. 2, lines 2-6 and col. 6, lines 15-17 and 32-34. However, De very specifically discloses that a forward body bias is applied to transistors 340 and 342 in an active mode of a NAND gate 336. See col. 6, lines 17- 21. De's active mode of NAND gate 336 does not correspond to the claimed "when the SRAM memory device is in a STANDBY mode."

Additionally, De's col. 6, lines 25-29 relating to a standby mode of a NAND gate 336 does not suggest a forward body bias. De does not teach or suggest to apply a forward

body bias when a SRAM device is in a STANDBY mode. De relates to a NAND gate circuit 336 and how to apply body biases (such as via a voltage control circuitry 356). See De's col. 6, lines 12-15. De does not suggest the specific features of the bias transistor, the forward body bias and "when the SRAM memory device is in the STANDBY mode." De also does not teach or suggest that a gate of a bias transistor to receive a STANDBY signal indicative of the STANDBY mode of the SRAM memory device. Therefore, the Office Action's alleged combination with De is improper.

Applicants respectfully submit that Matsumura may not be combined with Sano and/or De so as to teach or suggest to apply a forward body bias when the SRAM memory device is in the STANDBY mode, as recited in independent claim 1. The Office Action's combination of references is based on impermissible hindsight since there is no suggestion for the combination. De's description of a forward bias may not be combined with Matsumura/Sano as alleged so as to reach the features of independent claim 1.

For at least the reasons set forth above, Matsumura, Sano and De do not teach or suggest all the features of independent claim 1. Thus, independent claim 1 defines patentable subject matter

Independent claim 9 recites a first SRAM memory cell and a supply voltage line to provide a first supply voltage to two transistors of the at least four transistors of the first SRAM memory cell when the first SRAM memory cell is in an ACTIVE mode and to provide a second supply voltage to the two transistors when the first SRAM memory cell is in a STANDBY mode, the second supply voltage being different than the first supply voltage.

Independent claim 9 also recites a switching device to apply a forward body bias to the two transistors of the cross-coupled inverter configuration of the first SRAM memory cell when the first SRAM memory cell is in the STANDBY mode. Independent claim 9 also recites the switching device comprises an NMOS transistor having a source coupled to GROUND and a gate coupled to a power control unit, and wherein a gate of the NMOS transistor to receive a STANDBY signal from the power control unit indicative of the STANDBY mode of the first SRAM memory cell.

For at least similar reasons as set forth above, the applied references do not teach or suggest at least these features of independent claim 9. The applied references do not teach or suggest to apply a forward body bias when the first SRAM memory cell is in the STANDBY mode, alone or in combination with the claimed features that switching device comprises an NMOS transistor having a source coupled to GROUND and a gate coupled to a power control unit, and wherein a gate of the NMOS transistor to receive a STANDBY signal from the power control unit indicative of the STANDBY mode of the first SRAM memory cell. Matsumura and the other applied references also do not teach or suggest the supply voltage line to provide a first supply voltage and a second supply voltage in combination with the claimed two transistors. Thus, independent claim 9 defines patentable subject matter.

Independent claim 18 recites a static random access memory (SRAM) device and a power control unit to control a supply voltage level applied to the SRAM device and to provide a signal indicative of a mode of the SRAM device, the power control unit to apply a

first voltage level when the signal indicates that the SRAM device is in an ACTIVE mode and to apply a second voltage level when the signal indicates that the SRAM device is in a STANDBY mode. Independent claim 18 also recites that the SRAM device includes a switching device to apply a forward bias to transistors within the SRAM device when the signal provided by the power control unit indicates the STANDBY mode of the SRAM device.

For at least similar reasons as set forth above, the applied references do not teach or suggest at least these features of independent claim 18. The applied references do not teach or suggest to apply a forward bias when a signal provided by the power control unit indicates the STANDBY mode of the SRAM device. The applied references also do not teach or suggest to apply a first voltage level when the signal indicates that the SRAM device is in an ACTIVE mode and to apply a second voltage level when the signal indicates that the SRAM device is in a STANDBY mode. Thus, independent claim 18 defines patentable subject matter.

For at least the reasons set forth above, each of independent claims 1, 9 and 18 define patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-3, 7-11, 13, 15-20, 24-26, 29-30 and 33-37 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
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